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F-B200GL NB-IoT Module Hardware Design Manual

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Product Appearance

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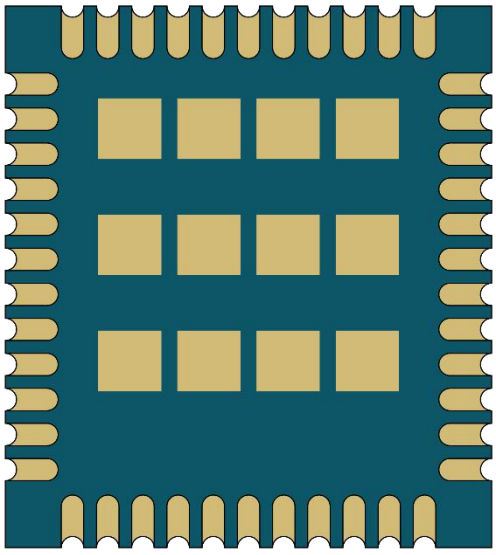

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Chapter1 Product Overview

1.1 F-B200GL Summary

F-B200GL is an LTE Cat.NB1 mode wireless communication module that supports half duplex LTE, but does not support the function of diversity receive. It can provide data connection through NB-IoT network.

F-B200GL supports band and BT function are shown as follows.

Form 1-1 Band and BT Function

Module	LTE Band	Diversity Reception	BT
F-B200GL	Cat NB1: LTE-FDD: B3/B5/B8	Nonsupport	TBD

F-B200GL has a 15.2mm x 17.0mm x 2.6mm compact size, which can meet almost all the M2M application, including automobile and personal tracking service, wearable service, security systems, wireless POS machine, industrial-grade PDA, smart meter, wireless remote control, etc.

F-B200GL is a SMD type module with 58 LCC pads, which can be easily embedded into other products. It integrates many network protocols such as TCP, UDP, CoAP, MQTT, LWM2M and the extended extension AT command makes these Internet protocols easier for users.

1.2 Main Performance

Form 1-2 Main Performance Parameters

Functions	Description
Power Supply	Power supply range: 3.3V ~ 4.3V. Typical power supply: 3.8V.
Power Class	Class 3 (23dBm±2.7dB) for LTE-FDD. Class 3 (23dBm±2.7dB) for LTE-TDD.
LTE Features	Support LTE Cat.NB1. Support 200KHz bandwidth under LTE Cat.NB1. Support SISO of downlink Cat.NB1: Maximum uplink rate is 70kbps Maximum downlink rate is 32kbps
Network Protocol	Support PPP/TCP/UDP/COAP/MQTT/LWM2M/SSL/TLS/FTP(S)/HTTP(S). Support PAP (Password Authentication Protocol) and

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	CHAP (Challenge Handshake Authentication Protocol).
SMS	Text and PDU mode. Point-to-point messaging* SMS community broadcast* SMS storage: (U)SIM card default
(U)SIM Card	Support USIM/SIM card: power supply is 1.8V and 2.85V
UART Interface	**UART1**: Used for AT command and data transfer Default baud rate is 57600bps **UART2**: Reserved **UART3**: Reserved **UART4**: Used for software download, Module debug and log output
AT Command	The commands defined by 3GPP TS 27.007 and 3GPP TS 27.005, and add the new commands from Xiamen Four-Faith Technology
Antenna Interface	Include the main antenna interface (ANT_MAIN) and the BT antenna interface (ANT_BT)
Dimensions	(15.2±0.15) mm × (17.0±0.15) mm × (2.6±0. 2) mm
Operating Temperature	Normal operating temperature: -35℃ ~ +75℃ Extended operating temperature: -40℃ ~ +85℃
Software Upgrade	Upgrade software through UART or FOTA.
RoHS	All components completely conform to EU RoHS standard.

Note: "*" means in development.

1.3 RF Block Diagram

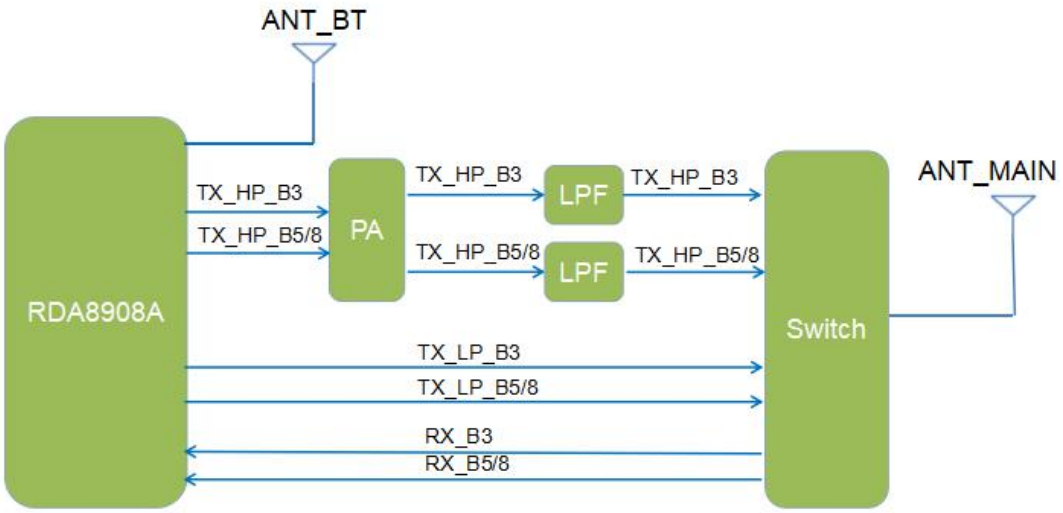

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Figure 1-1 F-B200GL- RF Block Diagram

Chapter2 Application Interfaces

F-B200GL is an LCC footprint with 58 pins which can be used to wireless application platform and provide a functional interface as follows:

1. Power supply interface
2. (U)SIM card interface
3. UART interface
4. I^2C interface
5. SPI interface

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2.1 Pin Assignments

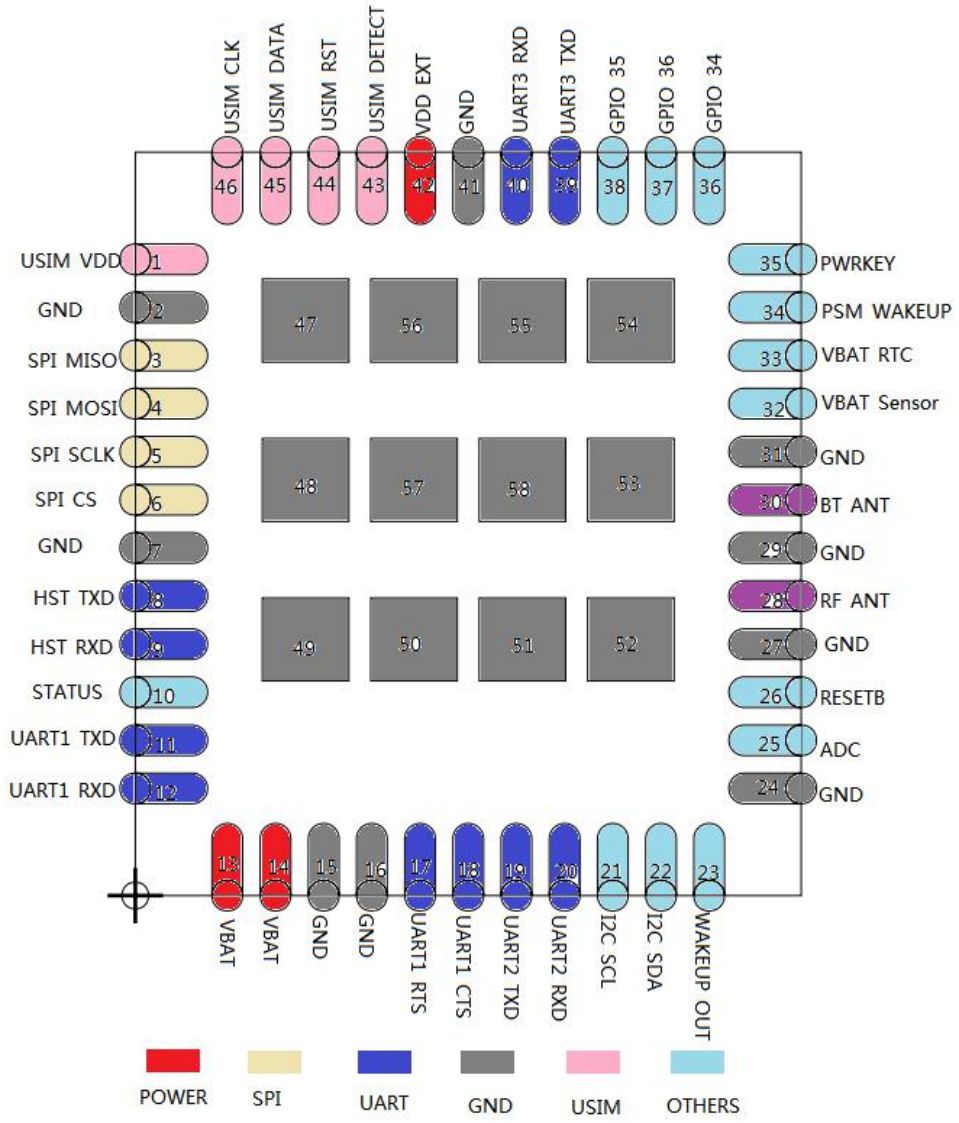

Figure 2-1 F-B200GL - Pin Assignments

NOTES:

1. All the RESERVED and unused pins need to float
2. GND pins need to connect to ground
3. Due to diode drop of chipset inside, The PWRKEY pin will output 1.0V

2.2 I/O Definition

Form 2-1 I/O Definition

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Symbol	Description
IO	IN/OUT dual-port
DI	Digital input
DO	Digital output
PI	Power input
PO	Power output
AI	Analog input
AO	Analog output
OD	Open-drain

2.3 Pin Descriptions

Form 2-2 Pin Descriptions

Power Supply				
Pad #	**Pad Name**	**I/O**	**Description**	**Remark**
13, 14	VBAT	PI	Power supply for module	3.4~4.2V
42	VDD_EXT	PO	Output 1.8/2.8V	Pull up only for external GPIOS; unused state: float.
7, 15, 16, 24, 27, 29, 31, 41, 47~58	GND		Ground	
Module on/off				
Pad #	**Pad Name**	**I/O**	**Description**	**Remark**
35	PWRKEY	DI	Turn on/off signal	
26	RESET_N	DI	Reset signal	Unused state: float.
Status indication				
Pad #	**Pad Name**	**I/O**	**Description**	**Remark**
10	STATUS	DO	Indicates working state	VDD_EXT power domain, unused state: float.
GPIO interface				
Pad #	**Pad Name**	**I/O**	**Description**	**Remark**
37	GPIO_36	IO	General purpose input/output	VDD_EXT power domain, unused state: float.
36	GPIO_34	IO	General purpose input/output	VDD_EXT power domain, unused state: float.

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38	GPIO_35	IO	General purpose input/output	VDD_EXT power domain, unused state: float.

(U)SIM card interface				
Pad #	**Pad Name**	**I/O**	**Description**	**Remark**
43	USIM_PRESENCE	DI	(U)SIM card detection	VDD_EXT power domain, unused state: float.
1	USIM_VDD	PO	(U)SIM card power supply	The module identification 1.8V or 2.85V automatically.
44	USIM_RST	DO	(U)SIM card reset line	
45	USIM_DATA	IO	(U)SIM card data line	
46	USIM_CLK	DO	(U)SIM card clock line	
2	USIM_GND		(U)SIM card specified ground	

UART1 interface				
Pad #	**Pad Name**	**I/O**	**Description**	**Remark**
12	UART1_RXD	DI	Data receive	VDD_EXT power domain, unused state: float.
11	UART1_TXD	DO	Data transmit	VDD_EXT power domain, unused state: float.
18	UART1_CTS	DO	Clear to send	VDD_EXT power domain, unused state: float.
17	UART1_RTS	DI	Require to send	VDD_EXT power domain, unused state: float.

UART2 interface				
Pad #	**Pad Name**	**I/O**	**Description**	**Remark**
19	UART2_TXD	DO	UART2_TXD, data transmit	VDD_EXT power domain, unused state: float.
20	UART2_RXD	DI	UART2_RXD, data receive	VDD_EXT power domain, unused state: float.

UART3 interface				
Pad #	**Pad Name**	**I/O**	**Description**	**Remark**
40	UART3_RXD	DI	Data transmit	VDD_EXT power domain, unused state: float.
39	UART3_TXD	DO	Data receive	VDD_EXT power domain, unused state: float.

UART4 interface				
Pad #	**Pad Name**	**I/O**	**Description**	**Remark**
9	HST_RXD	DI	Data receive	VDD_EXT power domain,

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				unused state: float.
8	HST_TXD	DO	Data transmit	VDD_EXT power domain, unused state: float.
SPI interface				
Pad #	**Pad Name**	**I/O**	**Description**	**Remark**
6	SPI_CS	DO	SPI chipset selection	VDD_EXT power domain, unused state: float.
5	SPI_CLK	IO	SPI clock	VDD_EXT power domain, unused state: float.
4	SPI_DI_0	IO	SPI data transmission	VDD_EXT power domain, unused state: float.
3	SPI_DI_1	IO	SPI data transmission	VDD_EXT power domain, unused state: float.
I2C interface				
Pad #	**Pad Name**	**I/O**	**Description**	**Remark**
21	I2C_SCL	OD	I2C serial clock	VDD_EXT power domain, unused state: float.
22	I2C_SDA	OD	I2C serial data	VDD_EXT power domain, unused state: float.
Antenna interface				
Pad #	**Pad Name**	**I/O**	**Description**	**Remark**
28	ANT_MAIN	IO	Main antenna interface	
30	ANT_BT	IO	BT antenna interface	Unused state: float.
Other pins				
Pad #	**Pad Name**	**I/O**	**Description**	**Remark**
34	WAKEUP_IN	DI	Wake-up module	1.08V power domain, enable it high level more than last 1s. It used on wakeup module in PSM mode.
23	WAKEUP_OUT	DO	Wakeup external device	VDD_EXT power domain, unused state: float.
32	V_BAT_SENSOR	DI	VBAT voltage detection	Need connect with VBAT
33	V_BAT_RTC	DO	LDO Output for VBAT_RTC	Only external GPS RTC power supply, no load capacity
ADC interface				

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Pad #	Pad Name	I/O	Description	Remark
25	ADC_IN	AI	General analog to digital interface	unused state: float.

2.4 Working Mode

Form 2-3 Working Mode

Mode		Introductions
Normal Work Mode	Idle	The software is working. The module registers on the network and can receive and send data.
	Talk / Data	The network connected normally. In this mode, the module power consumption depends on network setting and data transmission rate.
Extended Idle Mode Discontinuous Reception		Compared with PSM, the power consumption of e-I-DRX slightly higher than PSM, but the accessibility of downlink communication link is greatly improved. The module and core network negotiate the parameters related to e-I-DRX through attachment and TAU process.
Airplane Mode		AT+CFUN=4 command can make the module into airplane mode, and in this mode, the RF function is closed.
Minimum Functional Mode		Using AT+CFUN=0 command can make the module into Minimum Functional Mode with constant electricity. In this mode, the RF and (U)SIM card function are off, but the GPIOS and USB can still work.
PSM		The module can further reduce its power consumption by entering PSM mode. PSM is similar to the shutdown mode, but the module is still registered on the network. The module does not need to reattach and re-establish PDN connection after awakening from PSM mode.
Shutdown Mode		In this mode, the module out-off of power, serial port and USB port unable to access, software not running.

2.5 Low Power Consumption Mode

2.5.1 Extended Idle Mode Discontinuous Reception(e-I-DRX)

F-B200GL can make power consumption through the e-I-DRX mode. The power consumption of e-I-DRX slightly higher than PSM. But compared with PSM, the

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accessibility of downlink communication is greatly improved. The module and core network negotiate the correlative parameters of e-I-DRX through attachment and TAU processes.

If the module decides to request e-I-DRX, it will carry the e-I-DRX parameters by the attached request or the TAU request message, including the parameters related to DRX, etc.

The core network decides whether to accept the e-I-DRX activation request.

1. When accepted, the core network can provide different e-I-DRX parameters from the module request and also provide the length of paging time window to the module based on operator's strategy.
2. The module uses the normal DRX mechanism when the core network rejects the module's request or does not support e-I-DRX, there are no e-I-DRX parameters in the attached /TAU receiving the message.
   If the network support e-I-DRX, you can use the AT+CEDRXS=1 command to enable this function.

2.5.2 Airplane Mode

The RF function will be turned off when the F-B200GL module enters into airplane mode, and all related AT commands are not accessible. You can make the module into airplane mode by software.

You can send **AT+CFUN=<fun>** command into this mode. The parameters of **<fun>** can be set 0,1 or 4.

1. AT+CFUN=0: Minimum functional mode, RF and (U)SIM card are off.
2. AT+CFUN=1: all functions mode (default).
3. AT+CFUN=4: RF is off (airplane mode).

2.5.3 Power Save Mode (PSM)

PSM can make the power consumption lower. This mode is similar to power off, but the module is still connecting network. The module does not need to reattach and re-establish PDN connection after awakening from PSM mode. Therefore, it cannot immediately respond to the user request when the module enters into PSM.

When the module needs to use PSM, it will request an active time value during each attachment and TAU process. The network confirms the use of PSM by assigning active time values to the module if it supports PSM and accepts the module use of PSM. If the module wants to change the active time value, for example when the condition of the module changed, the module will request the required value in the TAU process.

If the network supports PSM, you can send the AT+CSCLK=2, AT+NVSETUP=2, AT+CPSMS=1 or AT+CPSMS=1 command to enable PSM.

When the module in PSM state, you can awaken the module under the following

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ways:

1. Pull the **PWRKEY** pin into high;
2. Waiting for timer (T3412) overflow, the module will wake up automatically.

2.6 Power Supply

2.6.1 Power Supply Interface

F-B200GL has two VBAT pins for external power supply.

Form 2-4 VBAT And Relevant Ground Pins

Pad #	Pad Name	I/O	Description	DC characteristic	Remark
13, 14	VBAT	PI	power supply for RF module	Vmax = 4.2V Vmin = 3.4V Vnorm =3.8V	
7,15,16,24,27, 29,31,41,47~58	GND		Ground		

2.6.2 Power Supply Reference Design

F-B200GL power supply range is 3.4-4.2V, need to ensure input voltage not less than 3.4V. To reduce voltage dropping, it is recommended to place a low ESR 100uF filter capacitor and three ceramic capacitors (100nF, 33pF and 10pF) near the VBAT pin. When the module connection external power supply, the line width of VBAT should not be less than 2mm. In general, when route VBAT, the line should be the longer, the wider.

In additional, it is recommended to add a 5.1V, more than 0.5W Zener diode at the front of the power supply for keeping the power supply stable. The reference design of the power supply circuit is as follows:

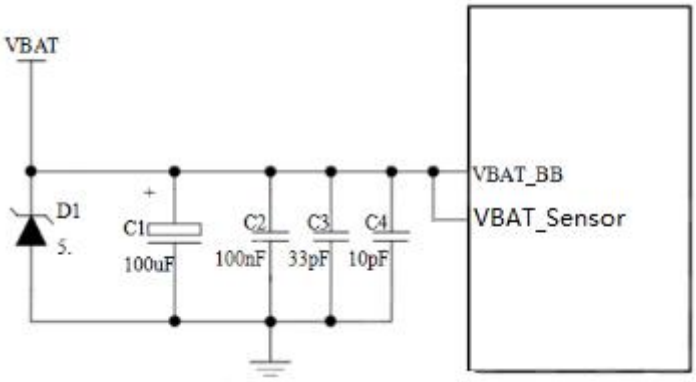

Figure 2-2 Power Supply Reference Design

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2.7 Module Startup/Shutdown

2.7.1 Startup

You can startup module by pulling down **PWRKEY** pin at least 480ms when the module in power off mode. It is recommended to use the open collector drive circuit to control the PWRKEY pin. You can release the PWRKEY pin after the STATUS pin is high.

Form 2-5 PWRKEY Pin Description

Pad #	Pin Name	Description	DC character	Remark
35	PWRKEY	Used for the module startup/shutdown	VIH max=2.1V VIH min=1.3V VIL max=0.5V	Due to diode voltage drop of chipset inside, this pin will output 1.0V

Reference Design:

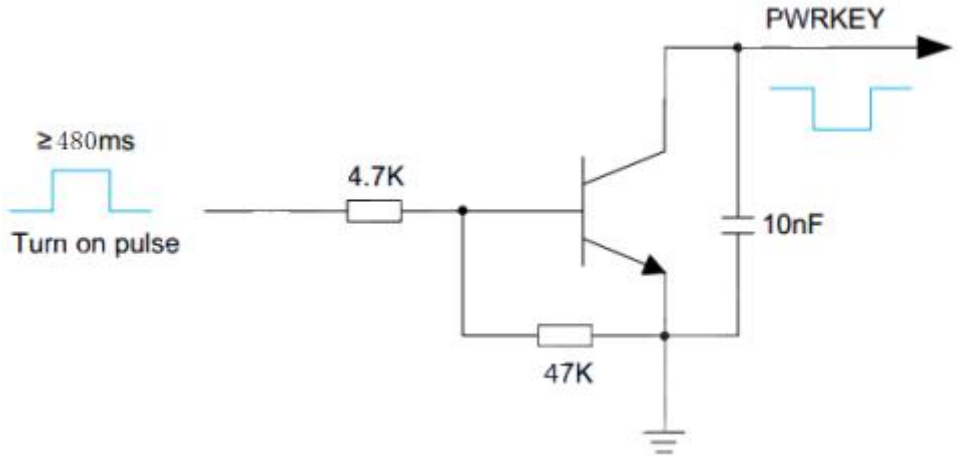

Figure 2-3 Open Collector Drive Circuit Reference

Another way to control **PWRKEY** pin is through a button switch directly. A TVS is placed near the button for ESD protection.

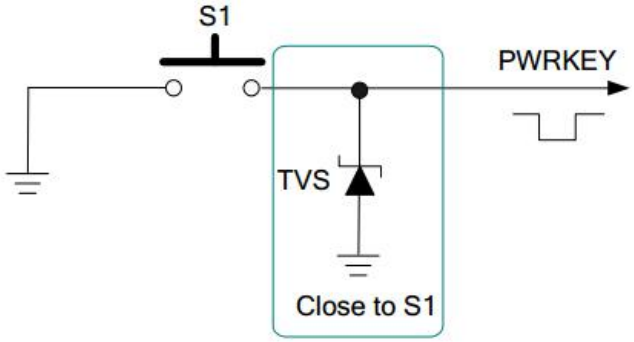

Figure 2-4 Button Startup Reference Circuit

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2.7.2 Shutdown

You can shutdown module by AT+CPOF command.

2.8 Module Reset

The RESET_N pin is used to reset the module. You can reset it by pulling down the RESET_N pin at least 950ms. The RESET_N signal is sensitive to interference, so it is recommended that the wiring on the interface board of the module should be as short as possible, and the trace should be surrounded by GND.

AT reset command: AT+TRB.

Form 2-6 RESET_N Pin Description

Pad #	Pad Name	I/O	Description	DC Characteristic	Remark
26	RESET_N	DI	Reset signal	V_{IH} max=2.1V V_{IH} min=1.3V	Unused state: float.

The reference circuit is similar to the PWRKEY control circuit, you can use an open collector drive circuit or a button to control the RESET_N pin, shown as follows:

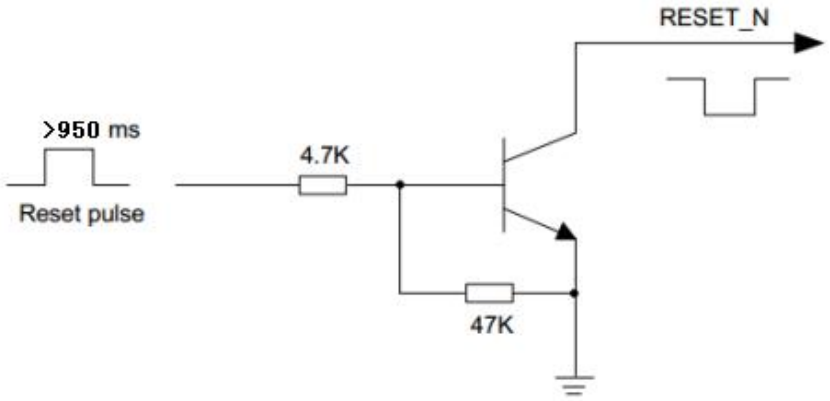

Figure 2-5 RESET_N Open Collector Drive Reference Reset Circuit

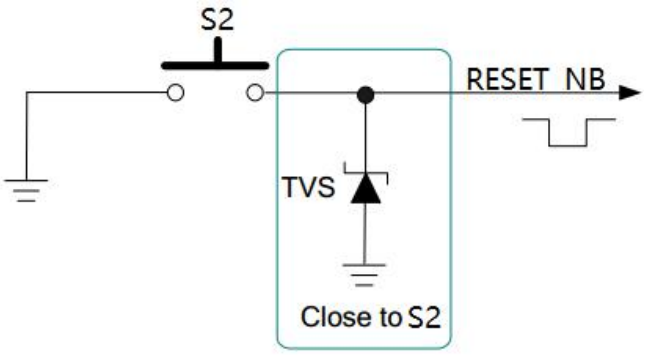

Figure 2-6 RESET_N Button Reset Reference Circuit

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2.9 (U)SIM Interface

The (U)SIM interface conforms to ETSI and IMT-2000 standard, support for 1.8V and 2.85V (U)SIM card.

Form 2-7 (U)SIM Pins Description

Pin No	Pin name	I/O	Description	Remark
43	USIM_DETECT	DI	(U)SIM insert in or out detection	
1	USIM_VDD	PO	(U)SIM power supply	Support 1.8V and 2.85V voltage
44	USIM_RST	DO	(U)SIM reset signal	
45	USIM_DATA	IO	(U)SIM data signal	
46	USIM_CLK	DO	(U)SIM clock signal	
2	USIM_GND		(U)SIM's dedicated GND	

The F-B200GL module can support (U)SIM card hot plug function and support high and low levels detection through the USIM_DETECT pin. This function is closed by default.

The 8-pin (U)SIM connector reference circuit design as follows:

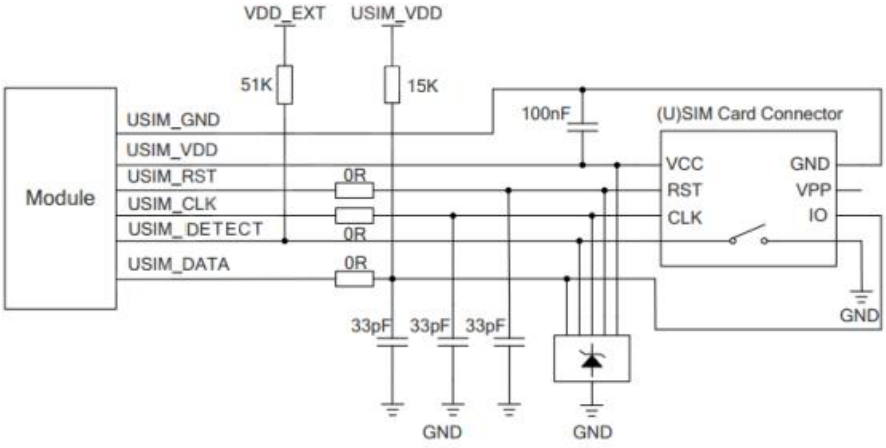

Figure 2-7 8-pin (U)SIM Connector Reference Circuit Design

If you do not need the USIM_PRESENCE pin to detect (U)SIM card, please keep it float. The reference circuit as follows:

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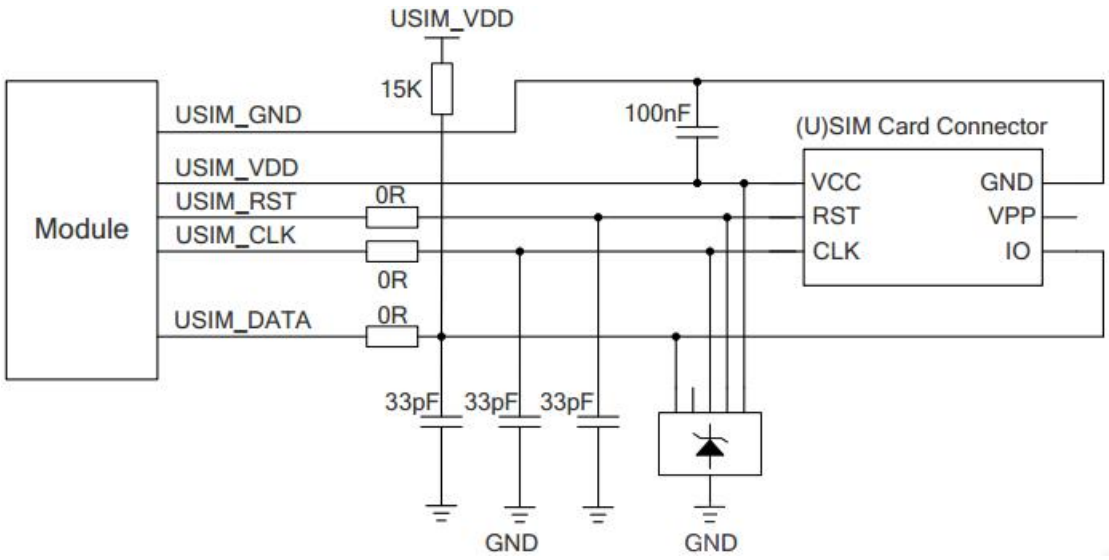

Figure 2-8 6-pin (U)SIM Connector Reference Design

In the circuit design of (U)SIM interface, the following design principles are recommended in the circuit design to ensure the good performance and non-damage of (U)SIM card:

1. (U)SIM card connector is placed close to the module, and make sure the (U)SIM card signal line should not longer than 200mm.
2. (U)SIM card signal need to route away from the RF trace and the VBAT power trace.
3. The GND of (U)SIM card connector and the USIM_GND of the module are wiring should be short and thick; Ensure that the width of USIM_VDD and USIM_GND wiring is not less than 0.5mm, and the bypass capacitance between USIM_VDD and USIM_GND is not more than 1uF, and close to the USIM card connector; if the system is complete on the client motherboard, the USIM_GND can connect directly to the system ground.
4. In order to prevent the signal mutual crosstalk between the USIM_CLK and the USIM_DATA, they cannot route too close, and the ground-shielded should be add between the USIM_CLK and the USIM_DATA; otherwise, the USIM_RST signal also need to be protected by ground.
5. In order to ensure good ESD performance, it is recommended to add the TVS tube to (U)SIM card; The parasitic capacitance of TVS tube should not more than 15PF; For the convenience of debugging, it is recommended reserve series resistance is needed on the (U)SIM signal line of the module; The peripheral components of the (U)SIM card should be placed as close as possible to the (U)SIM card connector;
6. The USIM_DATA, USIM_CLK and USIM_RST need add parallel 33pF capacitors which used to filter out the interference of RF, and these capacitors should be placed close to (U)SIM card connector.
7. The pull-up resistor of USIM_DATA can increase the antijamming capability of

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(U)SIM card. When the (U)SIM trace too long or the interference source is too close, pull-up resistor is recommended.

2.10 UART Interface

F-B200GL has 4 UATR interfaces: UART1, UART2, UART3 and UART4. The main features of these 4 UATR interfaces shown as follows:

1. UART1: Support 57600bps baud rate, used for AT command and data transmission.
2. UART2: Reserved.
3. UART3: Reserved.
4. UART4: Support 115200bps baud rate, used for module debug and log output.

Form 2-9 UART1 Pins Description

Pad #	Pad Name	I/O	Description	Remark
12	UART1_RXD	DI	Transmit data	VDD_EXT power domain, Unused state: float
11	UART1_TXD	DO	Receive data	VDD_EXT power domain, Unused state: float
18	UART1_CTS	DO	Send to clear	VDD_EXT power domain, Unused state: float
17	UART1_RTS	DI	Require send data	VDD_EXT power domain, Unused state: float

Form 2-10 UART2 Pins Description

Pad #	Pad Name	I/O	Description	Remark
19	UART2_TXD	DO	Transmit data	VDD_EXT power domain, Unused state: float
20	UART2_RXD	DI	Receive data	VDD_EXT power domain, Unused state: float

Form 2-11 UART3 Pins Description

Pad #	Pad Name	I/O	Description	Remark
40	UART3_RXD	DO	Receive data	VDD_EXT power domain, Unused state: float
39	UART3_TXD	DI	Transmit data	VDD_EXT power domain, Unused state: float

Form 2-12 UART4 Pins Description

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Pad #	Pad Name	I/O	Description	Remark
9	HST_RXD	DI	Receive data	VDD_EXT power domain, Unused state: float.
8	HST_TXD	DO	Transmit data	VDD_EXT power domain, Unused state: float.

The UART logic level is shown as follows:

Form 2-13 The Serial Logic Electrical Level

Parameter	Min	Max	Unit
V_{IL}	-0.3	0.6	V
V_{IH}	1.2	2.0	V
V_{OL}	0	0.45	V
V_{OH}	1.35	1.8	V

The UART voltage of F-B200GL is 1.8V/2.8V, so if the customer host system level is 3.3V, it is necessary to add a level converter in the serial port connection between the module and the host. The converter device recommended the TXS0108EPWR of TI company. The level conversion chip reference circuit design as follows:

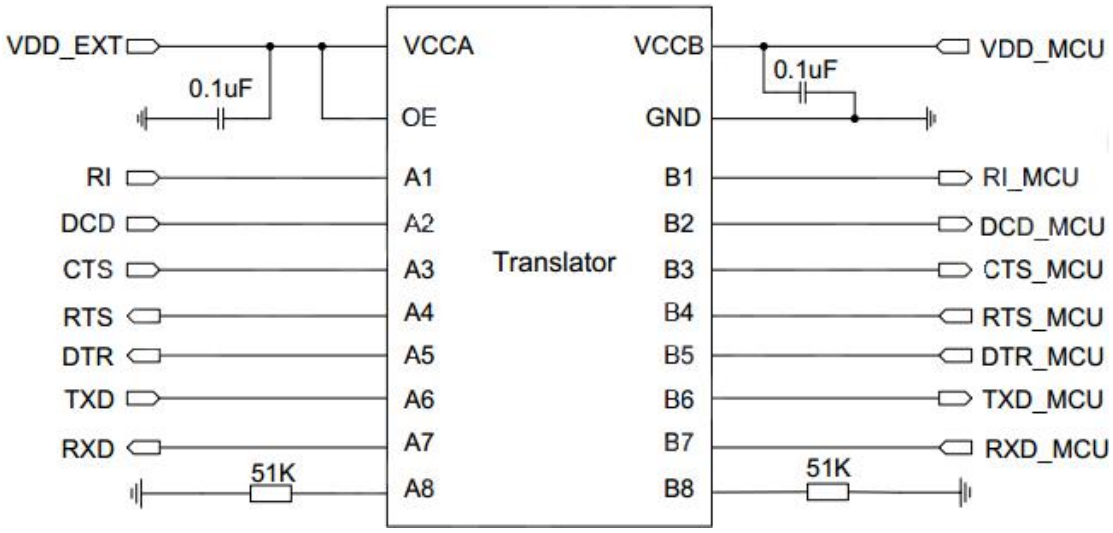

Figure 2-10 The Level Conversion Chip Reference Circuit

Another level conversion reference circuit design as follows. (notice: The input and output circuit design of the dotted line part can refer to the real line part, but the connection direction should be paid attention)

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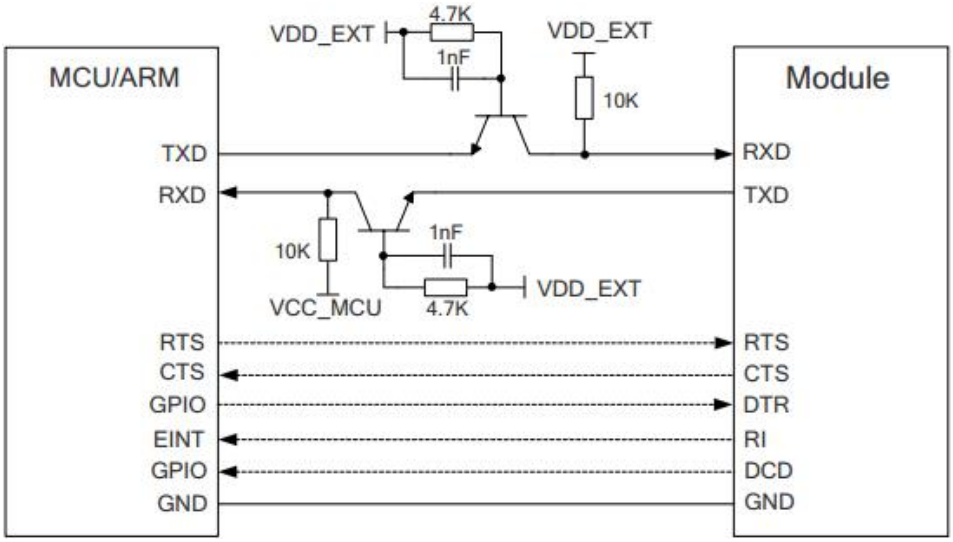

Figure 2-10 The Level Conversion Chip Reference Circuit

2.11 I2C Interface

I2C interface need to pull up 10K resistance.

Pad #	Name	I/O	Description	Remark
21	I2C_SCL	OD	I2C serial clock	VDD_EXT power domain, Unused state: float.
22	I2C_SDA	OD	I2C serial data	VDD_EXT power domain, Unused state: float.

2.12 Module Status Indication

The STATUS pin is used to indicate the module working state. The STATUS will output high level when the module turns on normally.

Form 2-14 STATUS Pin Description

Pad #	Pad Name	I/O	Description	Remark
20	STATUS	DO	Working status indication	1.8V power domain

Reference Design:

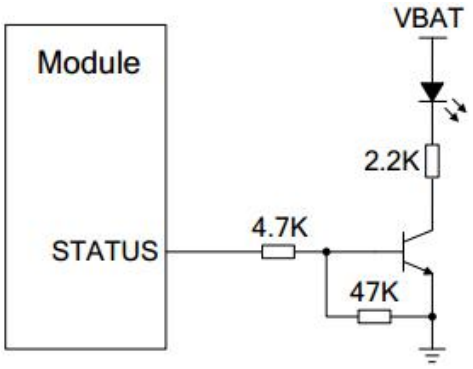

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Figure2-11 STATUS Reference Design

Chapter3 BT Function

TBD (nonsupport currently).

Chapter4 Antenna interface

F-B200GL supports one main antenna interface and one BT antenna interface, and the antenna interface has 50Ω impedance.

4.1 Main Antenna Interface

4.1.1 Pin Description

Form 4-1 Main Antenna Pin Description

Pin No	Pin name	I/O	Description	DC Character
28	ANT_MAIN	IO	Main antenna interface	50Ω characteristic impedance

4.1.2 Working Frequency Band

Form 4-2 Module Working Frequency Band

Frequency Band	F_{UL_low} - F_{UL_high}	F_{DL_low} - F_{DL_high}	Unit
LTE-FDD B1	1920~1980	2110~2170	MHz
LTE-FDD B3	1710~1785	1805~1880	MHz
LTE-FDD B5	824~849	869~894	MHz
LTE-FDD B8	880~915	925~960	MHz
LTE-FDD B20	832~862	791~821	MHz
LTE-FDD B28	703~748	758~803	MHz

4.1.3 Main Antenna Reference Design

In order to the regulation of RF performance better, it is recommended to reserve the π-type marching circuit. The π-type matched components (R1/C1/C2) should be

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placed as close to the antenna as possible.C1, C2 is default not to stick, only stick R1(0Ω resistance).

The reference circuit as follows:

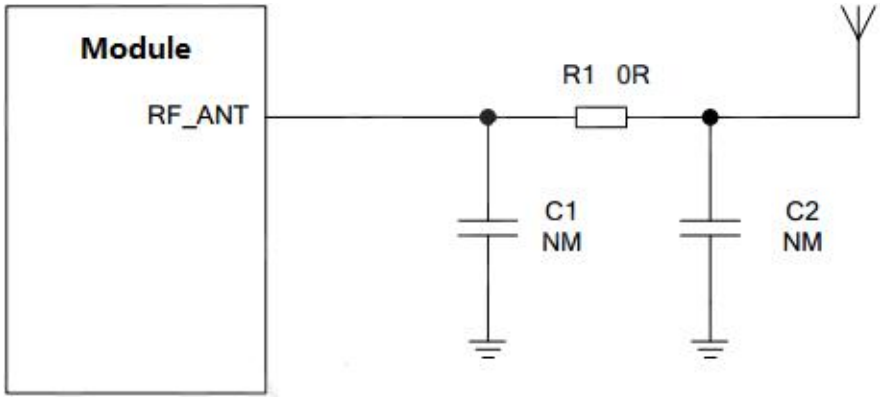

Figure4-1 RF_ANT Reference Design

4.1.4 RF_ANT Layout Guideline

All the RF signal traces should be kept the characteristic impedance at 50Ω, and the impedance depends on substrate dielectric, trace width(W), ground separation(S) and substrate height(H). PCB characteristic impedance is usually controlled by the microstrip line and coplanar waveguide. In order to reflect design principles, below shows the microstrip line and coplanar waveguide structure design when the impedance controlled in 50Ω.

1.Complete structure of microstrip line

Figure 4-2 Two Layers PCB Microstrip Line Structure

2. Complete structure of coplanar waveguide

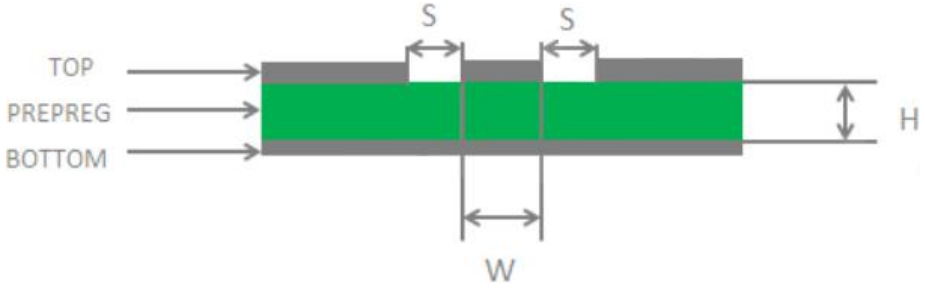

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Figure 4-3 Two Layers PCB Coplanar Waveguide Structure

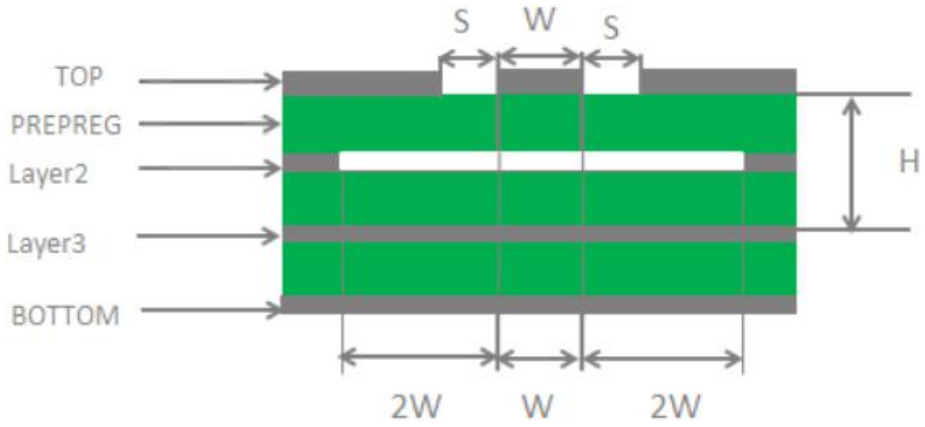

Figure 4-4 Four Layers PCB Coplanar Waveguide Structure (reference GND is layer3)

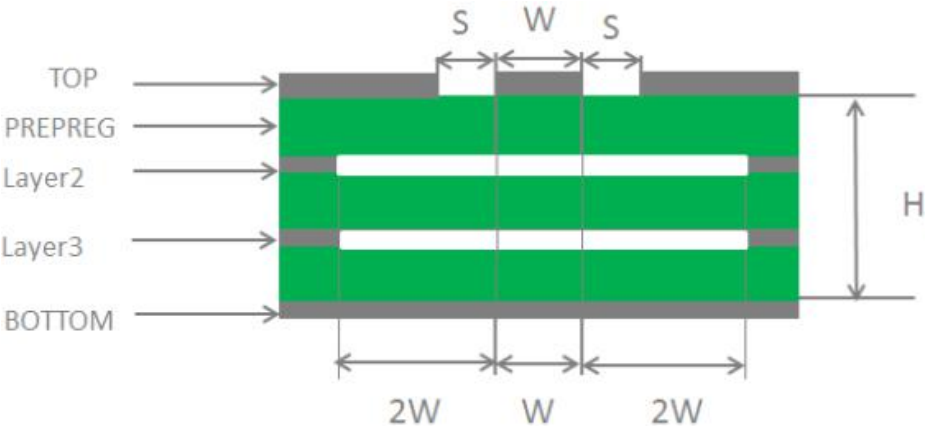

Figure 4-5 Four-layer PCB CPW Structure (reference GND is layer4)

In order to ensure good performance and reliability of the RF signals, the design principles of RF_ANT interface circuit are recommended as follows:

1. Should be used impedance simulation tools to accuracy-controlled impedance in 50Ω of the RF signal lines;
2. The GND pin adjacent to RF pins do not make the thermal pads, and should be fully in contact with the ground.
3. The distance between the RF pin and the RF connector shall be as short as possible, and avoid the right angle trace, it is recommended trace angle is 135 degrees.
4. When the connection device package is set up, it should be noted that the signal pin should be kept at a certain distance from the ground.
5. The ground plane of the RF signal lines reference should be complete; Adding a certain amount of ground holes around the signal line and reference ground can help improve the RF performance; The distance between the ground hole

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and the signal line should be at least double the line width (2*W).

4.2 BT Antenna Interface

4.2.1 Pin Description

Form 4-3 BT Antenna Pins Definition

Pad #	Pad Name	I/O	Description	DC Characteristic	Remark
30	ANT_BT	IO	BT antenna interface	50Ω impedance	Unused state: float.

4.2.2 BT Antenna Interface Reference Design

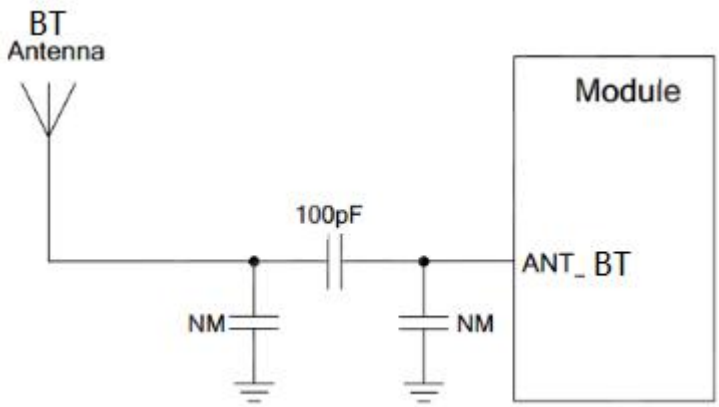

Figure 4-6 BT Antenna Interface Reference Design

4.3 Antenna Connector

The requirement of main antenna and GNSS antenna are shown as follows:

Form 4-5 Antenna Requirement

Type	Requirement
NB Antenna	VSWR: ≤ 2 Gain(dBi): 1 Maximum input power: 50W Input impedance: 50Ω Polarization type: vertical direction Cable insert depletion: <1.0dB (LTE B5/B8) Cable insert depletion: <1.5dB (LTE B3)
BT Antenna	Frequency range: 2400~2500MHz

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VSWR: <2 (typical value)

The RF Connector recommend to use Hirose UF.L-R-SMT.

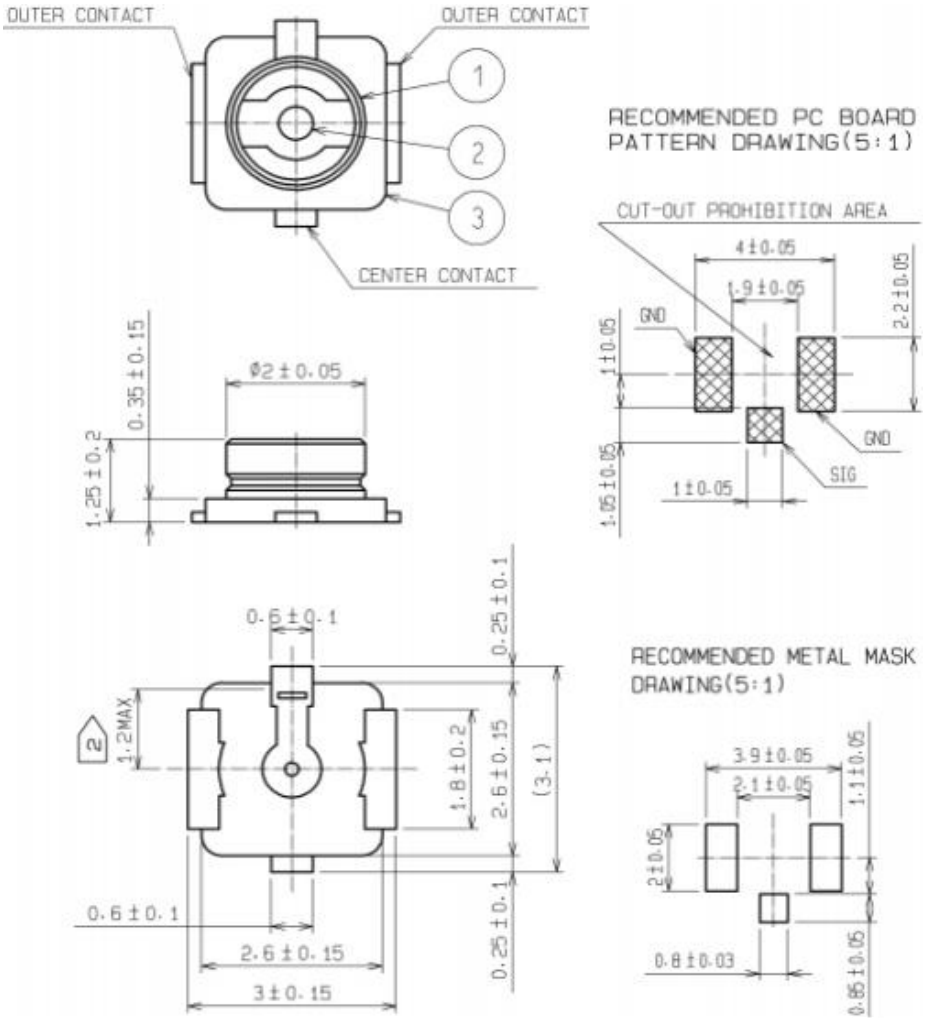

Figure 4-7 UF.L-R-SMT Connector Size(Unit: mm)

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Chapter5 Electrical Reliability and RF Performance

5.1 Absolute Maximum Rating

F-B200GL partial pins voltage and current maximum tolerance as follows:

Form 5-1 Absolute Maximum Rating

Parameter	Minimum	Maximum	Unit
VBAT		5	V

5.2 Power Supply

Form 5-2 The F-B200GL Power Supply

Parameter	Description	Condition	Minimum	Typical	Maximum	Unit
VBAT	Main power supply	The actual input voltage must be in this range.	3.4	3.8	4.2	V
I_{VBAT}	Peak current	LTE Cat.NB: Maximum output power is 23dBm.		170	TBD	mA

5.3 Operating Temperature

Form 5-3 Operating Temperature

Parameter	Minimum	Typical	Maximum	Unit
Normal operating temperature[1)]	-20	25	+70	℃
Extended operating temperature [2)]	-40		+85	℃

NOTICES:

1. [1)] It means that when the module working in this temperature range, the module's relevant performance meets the requirements of the 3GPP standard.
2. [2)] It means that when the module working in this temperature range, the module

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still keeping normally working status, and has the voice, short message, data transmission, emergency call etc. function. There will be no unrecoverable failures. The RF spectrum and network are almost unaffected. Only a few index parameters value may exceed the 3G standard such as output power, etc. When the temperature returns to the normal working temperature range, all indexes of the module still meet the 3GPP standard.

5.4 Power Consumption

Form 5-4 Power Consumption

Parameter	Description	Condition	Typical	Unit
I_{VBAT}	Power off	Power off mode	4.6	uA
	Minimum functional mode	AT+CFUN=0 (GPIOs and USB unconnected)	12.5	mA
	Power saving mode	PSM @LTE Cat.NB1 network	4	uA
	Standby mode	e-I-DRX=20.48s @LTE Cat.NB1 network (UART and USB do not connect)	0.78	mA
	LTE Cat.NB1 data transfer	23dBm (instrument test)	170	mA

5.5 Output Power

Form 5-5 Output Power

Frequency Band	Maximum	Minimum
LTE-FDD B3/B5/B8	23dBm±2.7dB	<-44dBm

5.6 Receive Sensitivity

Form 5-6 Receive Sensitivity

Band	Main Reception	Diversity Reception	Cat.NB1 Sensitivity 3GPP (dBm)
LTE-FDD B3	Support	Nonsupport	< -115
LTE-FDD B5	Support		< -115
LTE-FDD B8	Support		< -115

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5.7 Electronic Static Discharge (ESD)

In the application of module, it may cause certain damage to the module due to the ESD which generated between by human body and microelectronics, so the ESD protection should be taken seriously. The ESD protection should be adopted in the process of R&D, production assembly and testing, especially in product design, such as at the junction of the circuit design and the points susceptible to damage or influence by electrostatic discharge, anti-static protection should be added; anti-static gloves should be worn during production.

The ESD tolerance voltage of the important pin of the module as follows:

Form 5-7 ESD Performance Parameters

(Temperature: 25°C, Humidity: 45%)

Test Pins	Contact Discharge	Air Discharge	Unit
VBAT, GND	±10	±15	kV
Antenna	±10	±15	kV

Chapter6 Dimensions

This section describes the mechanical dimensions of the module. All dimensions in millimeter; All sizes without tolerance, the tolerance is ±0.15mm.

6.1 Module Dimensions

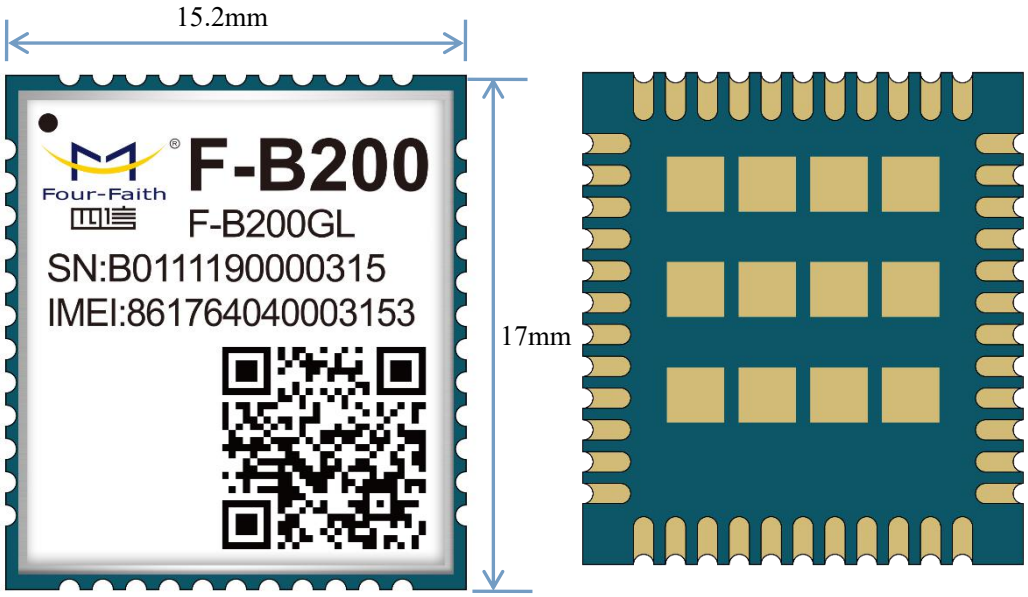

Figure 6-1 F-B200GL Top-View and Side-View

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6.2 Module Package

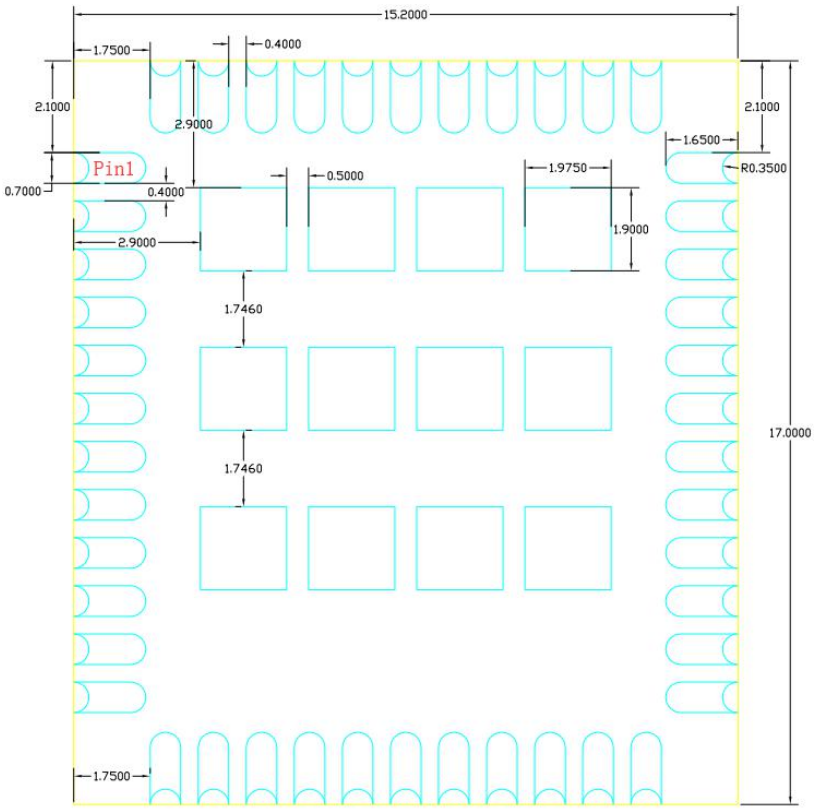

Figure 6-2 Module Package (Top View)

Chapter7 Storage and Production

7.1 Storage

F-B200GL packing in vacuum sealed bag, module storage conditions are shown as follows:

1. Temperature: ≤40°C and air humidity: ≤90%, modules can be stored in a vacuum sealed bag for 12 months.
2. After opening the vacuum sealed bag, if the following conditions are met, the module can directly carry out reflow soldering or other high temperature processes:
   - Storage air humidity: ≤10%.
   - Environmental temperature: ≤ 30°C, air humidity: ≤60%, finish SMD in 168 hours.
3. If the module is in the following conditions, it needs to be baked before the SMD:

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- Environmental temperature: 23°C(±5°C), air humidity: ≥10%.
- After opening the vacuum sealed bag, environmental temperature: ≤ 30°C, air humidity: ≤60%, cannot finish SMD in 168 hours.
- After opening the vacuum sealed bag, the module storage air humidity: ≥10%.

4. If the module needs to be baked, please bake it in 125°C(±5°C) for 48 hours.

NOTES:

The package of the module cannot withstand high temperature baking. So please remove the module package before the module baking. If it only takes a short time to bake, please reference the IPC/JEDECJ-STD-033 standard.

7.2 Product Welding

Use the printing scraper to print the solder paste on the screen plate, so that the solder paste can leak onto the PCB through the opening of the screen plate. And the strength of the printing scraper should be adjusted properly. In order to guarantee the quality of the printing paste, the thickness of the steel mesh corresponding to the F-B200GL module solder plate should be 0.18mm.

It is recommended temperature for reflow soldering is 235~245ºC, do not exceed 260ºC. In order to avoid repeated thermal damage to the module, it is recommended to paste the module after the first side of the PCB board completes the reflow welding. The recommended furnace temperature curves are shown as follows:

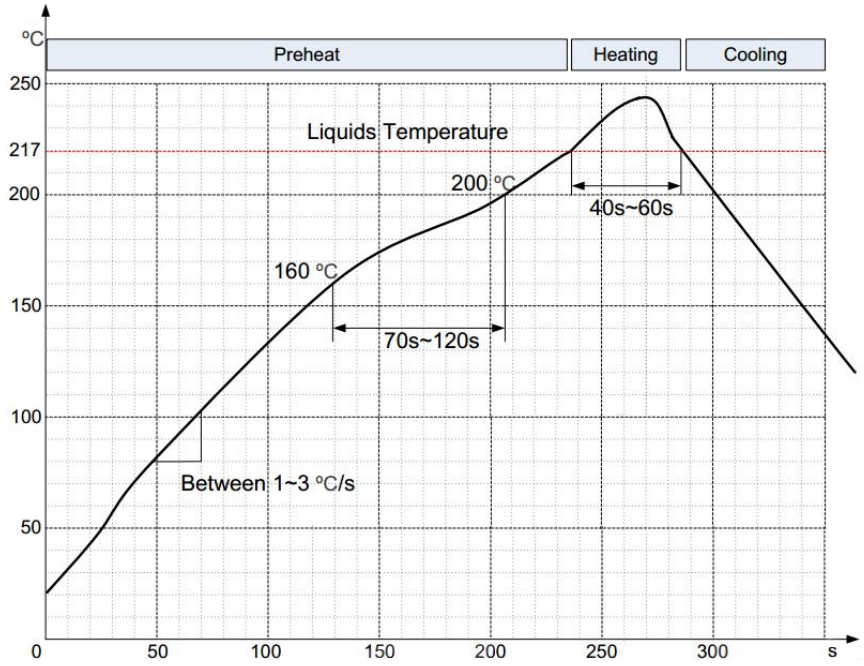

Figure 7-1 Reflow Temperature Curve

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7.3 Package

F-B200GL module is packaged in pallet and sealed in a vacuum sealing bag. It is recommended to open the vacuum packaging when actual production is used. Each pallet is 194.21mm long and 184.18mm width, include 49 F-B200GL modules. The pallet size is shown as follows:

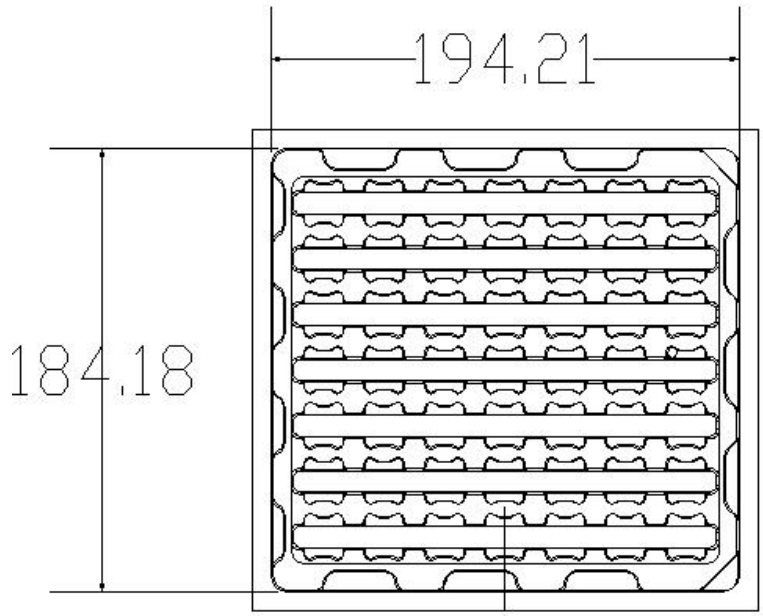

Figure 7-2 Pallet Size

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